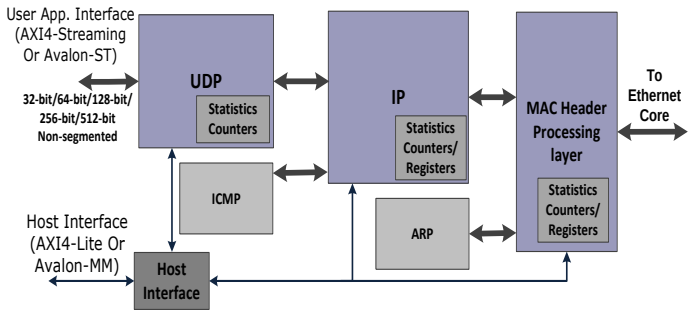
UDP/IP Offload Engine (UOE)

Product Brief (HTK-UOE-FPGA-aaa)

UOE is high performance and highly customizable UDP/IP hardware stack compliant with RFC 768 (for UDP) and RFC 791 (for IPv4)/RFC 2460(for IPv6). As shown in the figure below, the UOE core includes:

- L4 UDP engine
- L3 IPv4/IPv6 engine
- L2 Mac engine
- Statistic counter blocks and user configurable registers
- ARP and ICMP buffers



UOE is designed to be integrated with any Ethernet Solutions that has AXI4-ST/Avalon-ST interface. User interface can be customized for AXI4-ST or Avalon-ST. Data path in addition supports a wide range of interface widths from 32-bit up to 512-bit. Single clock design provides easy manageability for the user.

32-bit user interface runs @ 312.5MHz clock for 10G, 64-bit user interface runs @ 156.25MHz for 10G, 128-bit user interface runs @ 312.5MHz for 40G, 256-bit user interface runs @ 156.25MHz for 40G, and 512-bit user interface runs @ 312.5MHz for 100G.

Core IP layer can be customized for IPv4 or IPv6 depending on the application.

The header fields can be configured once for point-to-point applications.

Our solution implements and delivers the low latency with highest throughput and minimum or no inter-packet gap.

Key Features

- Implements RFC 768 for UDP.
- Implements RFC 791 for IPv4.
- Implements RFC 2460 for IPv6.
- Supports 32/64/128/256/512-bit wide data paths.
- Can handle data rate up to 100Gbps.
- Multiple user interface options for the data path; AXI4 streaming or Avalon Streaming
- Supports for VLAN tagged frames according to IEEE 802.1Q.
- Supports user data packets from 1 to 1472 bytes in standard mode.
- Optional Jumbo frames support up to 9000 bytes.
- High performance core with low latency and lowest inter-packet gaps.
- Remove padding from MAC frames.
- Discard datagrams having MAC errors, e.g. CRC error, PHY error.
- Can distinguish between unicast /multicast /broadcast datagrams and discard multicast packets.
- UDP checksum generation and checking at high speed using an efficient pipelined implementation.
- IPv4 checksum generation and checking and discard datagrams if checksum fails.
- Filtering of received frames based on MAC and IP address.
- Encapsulation/De-Encapsulation of MAC header along with UDP and IP
- Classify ARP and IP packets at L2
- Classify UDP and ICMP packets at L3
- Customizable IP layer for version 4 and 6.
- Can discard IP datagrams with invalid fragment offsets flags.
- Forward fragmented IP datagrams to fragment buffer after UDP and IP checksum checking and IP header sanity checks.
- Drops datagrams with invalid IP header fields.
- Implements statistics of frames, datagrams, segments at L2, L3 and L4 respectively.

Resource Utilization

The UOE core utilization summary is given in following tables.

UOE - Resource Usage for Xilinx Devices

Device	*User Interface (AXI4-ST)*	*Jumbo Frames Support*	*Slice LUTS*	*Slice Registers*	*BRAMs*
7-Series /UltraScale	32-Bit	No	*5,563*	*7,075*	*18K = 18; 36K = 1*
		Yes	*5,657*	7,150	*18K = 11; 36K = 20*
	64-Bit	No	*6,528*	8,241	*18K = 14; 36K = 5*
		Yes	*6,614*	8,316	*18K = 14; 36K = 17*
	128-Bit	No	*8,736*	10,570	*18K = 11; 36K = 9*
		Yes	*8,605*	10,621	*18K = 14; 36K = 17*
	256-Bit	No	*12,059*	15,301	*18K = 11; 36K = 17*
		Yes	*12,209*	15,336	*18K = 14; 36K = 17*
	512-Bit	No	*19,832*	25,664	*18K = 15; 36K = 29*
		Yes	*20,109*	25,690	*18K = 18; 36K = 29*

Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Altera) compiled (synthesized netlist) binary
- Other licensing options include:
  - Vendor and device family agnostic source code (Verilog) license

Ordering information

Following table lists the ordering code for the UOE IP Core.

UOE – Ordering Codes

Part #	*Description*
HTK-UOE-FPGA-32	32-bit data path UDP/IP core @ 312.5MHz clock for 10Gbps interface
HTK-UOE-FPGA-64	64-bit data path UDP/IP core @ 156.25MHz clock for 10Gbps interface
HTK-UOE-FPGA-128	128-bit data path UDP/IP core @ 312.5MHz clock for 40Gbps interface
HTK-UOE-FPGA-256	256-bit data path UDP/IP core @ 156.35MHz clock for 40Gbps interface
HTK-UOE-FPGA-512	512-bit data path UDP/IP core @ 312.5MHz clock for 100Gbps interface

Contact and Sales Information

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