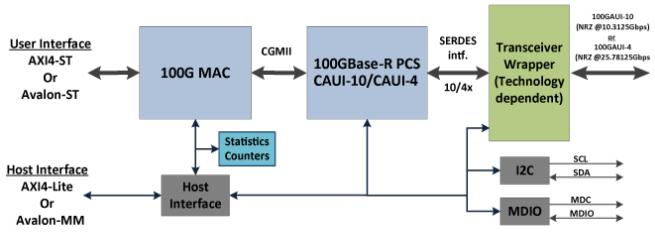
# 100 Gigabit Ethernet IP Solution

## Product Brief (HTK-100G-ETH-320-FPGA-Cxx)

The 100Gbps Ethernet IP solution offers a fully integrated IEEE802.3 compliant package for NIC (Network Interface Card) and Ethernet switching applications.
As shown in the figure below, the 100Gbps Ethernet IP includes:

- 100Gbps MAC core with AXI-4 Streaming or Avalon Streaming user interface.
- 100Gbps (100GBase-R) PCS core with support for CAUI-4 (-C4 option) and CAUI-10 (-C10 option) interfaces.
- RMON Block for statistics counters
- Technology dependent transceiver wrapper for Intel and/ or Xilinx FPGAs.
- Synthesizable packet generator/checker for quick bring up and standalone verification of 100G Ethernet solution.
- Linux based APIs/tools for configuration of the 100G core and getting various statistics.
- MDIO and I2C cores for optical module status and control.




## MAC Core Features

- Implements full 802.3 standard MAC layer with preamble/ SFD generation, CRC-32 generation and checking on transmit and receive paths respectively.
- Implements Deficit Idle Count (DIC) mechanism to ensure maximum possible throughput for transmit MAC while maintaining12byte average Inter Frame Gap (IFG).
- Implements RS layer functionality with start and terminate control characters alignment, error control character and fault sequence insertion and detection.
- Implements frame padding for packets less than 64 bytes on the transmit path and discards all frames less than 64 bytes (runt frames) on the receive path.
- Implements CRC-32 generation and checking at full 100Gbps rate.
- Implements a 320-bit CGMII interface (@312.5MHz)
- Implements 802.3bd specification with ability to generate and recognize PFC pause frames
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention. Non PFC mode only.
- Implements 802.3bd specification with ability to generate and recognize PFC pause frames
- Implements reconciliation sublayer functionality with start and terminate control characters alignment, error control character and fault sequence insertion and detection.
- Pause frame generation additionally controllable by user application offering flexible traffic flow control.
- Implements support for standard IEEE Ethernet length/type, 802.1Q VLAN tagged length/type and pause frames.
- Implements destination MAC address checking on receive path and accepts Unicast frames with matching destination MAC address only.
- Implements programmable promiscuous mode to accept all incoming traffic.
- Optional multicast address filtering with 64-bit HASH Filtering table providing imperfect filtering to reduce load on higher layers.
- Implements logic for optional padding removal on RX path for NIC applications or forwarding of unmodified data to the user interface.
- Implements sideband channel to provide per frame information to the user application on MAC receive path.
- Implements logic for optional forwarding of the CRC field to user application interface.
- Implements logic for optional forwarding of received pause frames to the user application interface.
- Implements sideband channel to provide per frame information to the user application on MAC receive path.
- Implements programmable maximum frame length support for standard Ethernet and Jumbo frames.
- Implements length error checking for standard Ethernet length frames and truncation of frames greater than programmed maximum frame length.
- Implements multiple statistics counters and per frame events for transmit and receive path such as good frames, CRC error, length error, remote/local fault etc.
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.
- Implements programmable internal CGMII Loop-back.
- Implements 512-bit AXI4/Avalon-ST streaming user application interface.
- Implements AXI4 or Avalon memory-mapped host interface for accessing the core's register file.

## PCS Core Features

- Implements 100GBase-R PCS core compliant with IEEE 802.3ba Specifications.
- Implements a 320-bit CGMII interface operating at 312.5MHz for 100G Ethernet.
- Implements optional Clause74 and Clause91 RS-FEC encoder, error correction and decoder.
- Implements 64b/66b encoding/decoding for transmit tand receive PCS.
- Implements 100G scrambling/descrambling using 802.3ba specified polynomial 1 + x39 + x58
- Implements Multi-Lane Distribution (MLD) across 20 Virtual Lanes (VLs)
- Implements periodic insertion of Alignment Marker(AM) on the transmit path and deletion on the receive path
- Implements 66-bit block synchronization and Alignment Marker Lock machines as specified in 802.3ba specifications.
- Implements lane reordering and deskew to align all PCS lanes and assemble an aggregate 100Gbps CGMII stream.
  Implements BIP-8 insertion/checking per Virtual Lane on transmit/receive respectively.
- Implements Inter Packet Gap (IPG) Insertion/Deletion for Alignment marker and clock compensation while maintaining a minimum of 1 byte IFG.
- Implements programmable internal remote CGMII loop-back which directs traffic received traffic back to transmit path.
- Implements Bit Error Rate (BER) monitor for monitoring excessive error ratio.
- Implements various configuration, status and statistics registers accessible through standard AXI4-Lite or Avalon-MM host interface.
- Implements gearbox logic to convert 66-bit blocks from 20 Virtual lanes to 10 physical lanes (CAUI-10) or 4 physical lanes (CAUI-4).

## Deliverables

- Encrypted MAC and PCS RTL for simulation and synthesis
- Encrypted L2 packet generator and checker RTL for simulation and synthesis
- Source code RTL (Verilog) for top level Ethernet wrappers to allow for user specific customizations.
- Technology specific transceiver wrappers for the selected device family
- Source code RTL (Verilog) for AXI4-Lite and Avalon-MM arbiters and address decoders
- Constraint files and synthesis scripts for reference design compilation
- Linux based APIs/tools to access core configuration and statistics registers
- Design guide(s) and user manual(s)

## Product Ordering Codes

HTK-100G-ETH-320-FPGA-C4: 100 Gigabit Ethernet Solution with 4 lane CAUI-4 PCS and optical side interface
HTK-100G-ETH-320-FPGA-C10: 100 Gigabit Ethernet Solution with 10 lane CAUI-10 PCS and optical side interface

## Links

https://hiteksys.com/fpga-ip-cores
https://hiteksys.com/fpga-ip-cores/100g-ethernet

## For sales or more information:

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## Resource Utilization

The core utilization summary for the 100G Ethernet solution is given in following tables. The Ethernet solution has been fully verified on different hardware platforms for both Intel and Xilinx FPGAs.

***100G Ethernet IP - Resource Usage for Xilinx Devices***

| Device | User Interface (AXI4) | Priority Flow Control (PFC) | PCS Type | Slice LUTS | Slice Registers | BRAMs |
|---|---|---|---|---|---|---|
| UltraScale/ UltraScale+ | 512-Bit (Non-Segmented) | No | **CAUI-4** | 51,837 | 62,022 | *18K = 4; 36K = 74* |
| | | Yes | **CAUI-4** | 52,300 | 62,673 | *18K = 4; 36K = 74* |
| | | No | CAUI-10 | 43,891 | 58,365 | *18K = 4; 36K = 74* |
| | | Yes | CAUI-10 | 44,354 | 59,016 | *18K = 4; 36K = 74* |
| 7-Series | 512-Bit (Non-Segmented) | No | **CAUI-4** | 51,899 | 61,984 | *18K = 4; 36K = 74* |
| | | Yes | **CAUI-4** | 52,349 | 62,635 | *18K = 4; 36K = 74* |
| | | No | CAUI-10 | 44,443 | 58,344 | *18K = 4; 36K = 74* |
| | | Yes | CAUI-10 | 44,893 | 58,995 | *18K = 4; 36K = 74* |

**Note:**

- *Register based RMON statistics block adds additional 1948 Slice LUTs and 1807 Slice Registers.*
- *CAUI-4 supported for devices with 25Gbps transceivers only.*

***100G Ethernet IP - Resource Usage for Intel Devices***

| Device | User Interface (Avalon) | Priority Flow Control (PFC) | PCS Type | COMB. ALUTs | Registers | Memory Blocks |
|---|---|---|---|---|---|---|
| Arria 10 | 512-Bit (Non-Segmented) | No | **CAUI-4** | 56,564 | 60,336 | M20K = 149 |
| | | Yes | **CAUI-4** | 56,966 | 61,009 | M20K = 149 |
| | | No | CAUI-10 | 37,804 | 55,349 | M20K = 149 |
| | | Yes | CAUI-10 | 38,206 | 56,022 | M20K = 149 |
| Stratix V | 512-Bit (Non-Segmented) | No | **CAUI-4** | 56,583 | 60,234 | M20K = 149 |
| | | Yes | **CAUI-4** | 56,988 | 60,824 | M20K = 149 |
| | | No | CAUI-10 | 37,802 | 55,163 | M20K = 149 |
| | | Yes | CAUI-10 | 38,297 | 55,753 | M20K = 149 |
| Stratix10 | 512-Bit (Non-Segmented) | No | **CAUI-4** | 59,177 | 73,177 | M20K = 148 |
| | | Yes | **CAUI-4** | 59,610 | 73,805 | M20K = 148 |

**Note:**

- Register based *RMON statistics block adds additional 2000 Comb. ALUTs and 1800 Registers.*
- *CAUI-4 supported for devices with 25Gbps transceivers only.*