HITEK SYSTEMS

100Gbps Ethernet Solution

(MAC and 100GBase-R PCS Cores)

[HTK-100G-ETH-320-FPGA]

Interoperability and Verification Report

March 06, 2012

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REVISION HISTORY

Revision	*Date of Issue*	*Author*	*Scope*
0.1	02/24/2012	HT	- Initial version
1.0	02/06/2012	HT/TM	Updated with the test results

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1. INTRODUCTION

This report documents the results for the interoperability and verification results for Hitek's 100G Ethernet solution, HTK-100G-ETH-320-FPGA. The 100Gbps Ethernet IP solution offers a fully integrated IEEE802.3ba compliant package for NIC (Network Interface Card) and Ethernet switching applications. The 100Gbps Ethernet IP solution includes:

- 100Gbps MAC core
- 100Gbps (100GBase-R) PCS core
- Technology dependent transceiver wrapper for Altera and/or Xilinx FPGAs
- Statistics counter block (for RMON and MIB)
- MDIO and I2C cores for optical module status and control

1.1. Overview

The verification tests for the 100G Ethernet solution are divided into three main sections:

1. Interoperability tests
2. PCS layer tests
3. MAC layer tests

Beside the basic interoperability and verification testing at the logical level, emphasis has also been placed into testing the clock compensation mechanism of the 100G Ethernet cores. Operation of the Ethernet cores has been validated with a maximum clock frequency deviation of +/-200PPM between the DUT and the testing station.

1.2. Test Setup

Following figure shows the setup used for the 100G interoperability and verification testing.

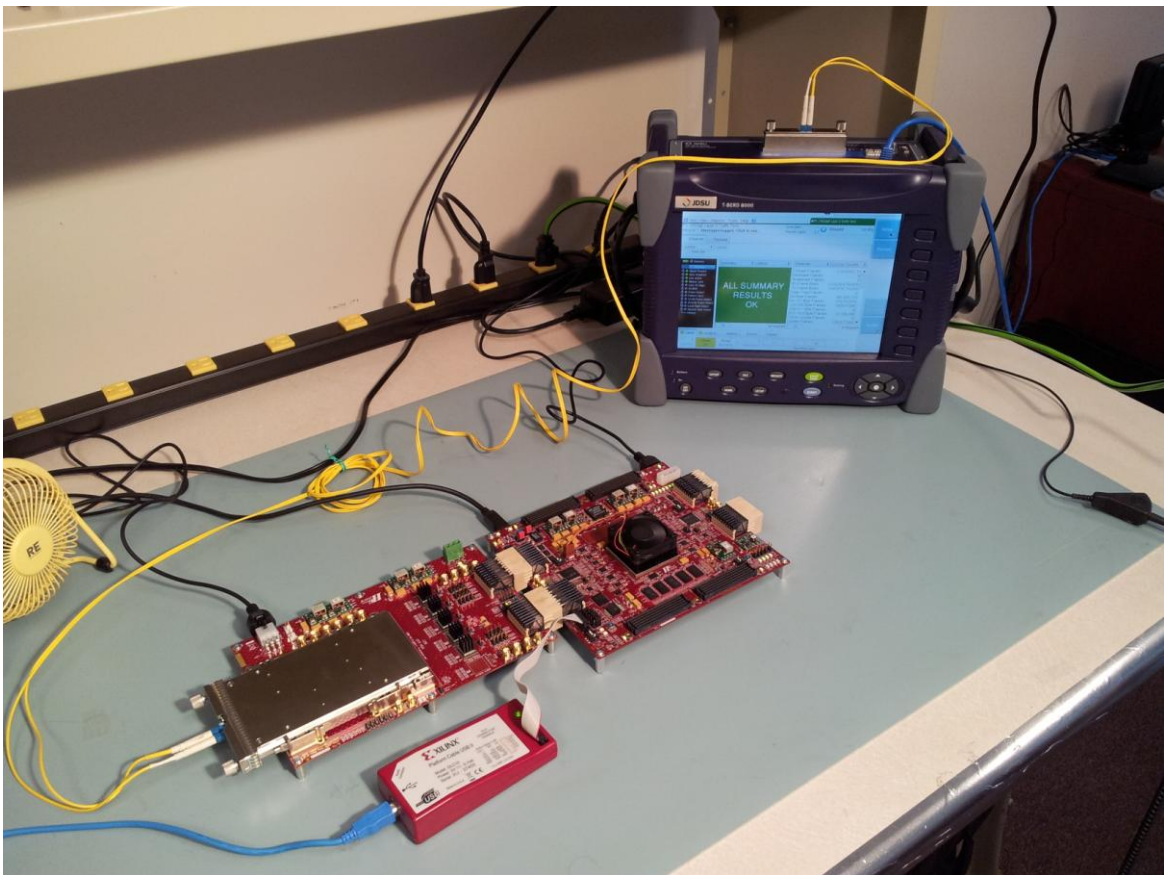


Figure 1. Verification Test Setup

As shown in the figure below, the interoperability and verification test setup is composed of the following elements:

1. DUT for the 100Gbps based upon the following modules:
   a. HTG-V6HXT-100G FPGA module with Xilinx XC6VHX565T-2 (**mid speed grade**) FPGA with AirMax connectors for bi-directional links to the FPGAs 12.5Gbps GTH transceivers and control signals
   b. HTG-CFP-MDL-PRO CFP carrier module with 5 Netlogic's dual-channel EDC/re-timers, CFP cage and AirMax connectors for bi-directional links to the FPGA module
   c. Santur PD100-TXLD 10x10 SMF 100G CFP plugged into carrier module with a single mode fiber interface to Ethernet tester. (Note: interoperability testing also performed with the Reflex Photonics10x10 CF-x12-C11901 inter-board parallel optics modules)
2. 100G/40G Ethernet tester (Testing Station); a JDSU TBird-8000 with 100G/40G Ethernet interface option and Santur PD100-TXLD 10x10 SMF 100G CFP connected to the DUT
3. Windows PC to host the GUI controlling the DUT

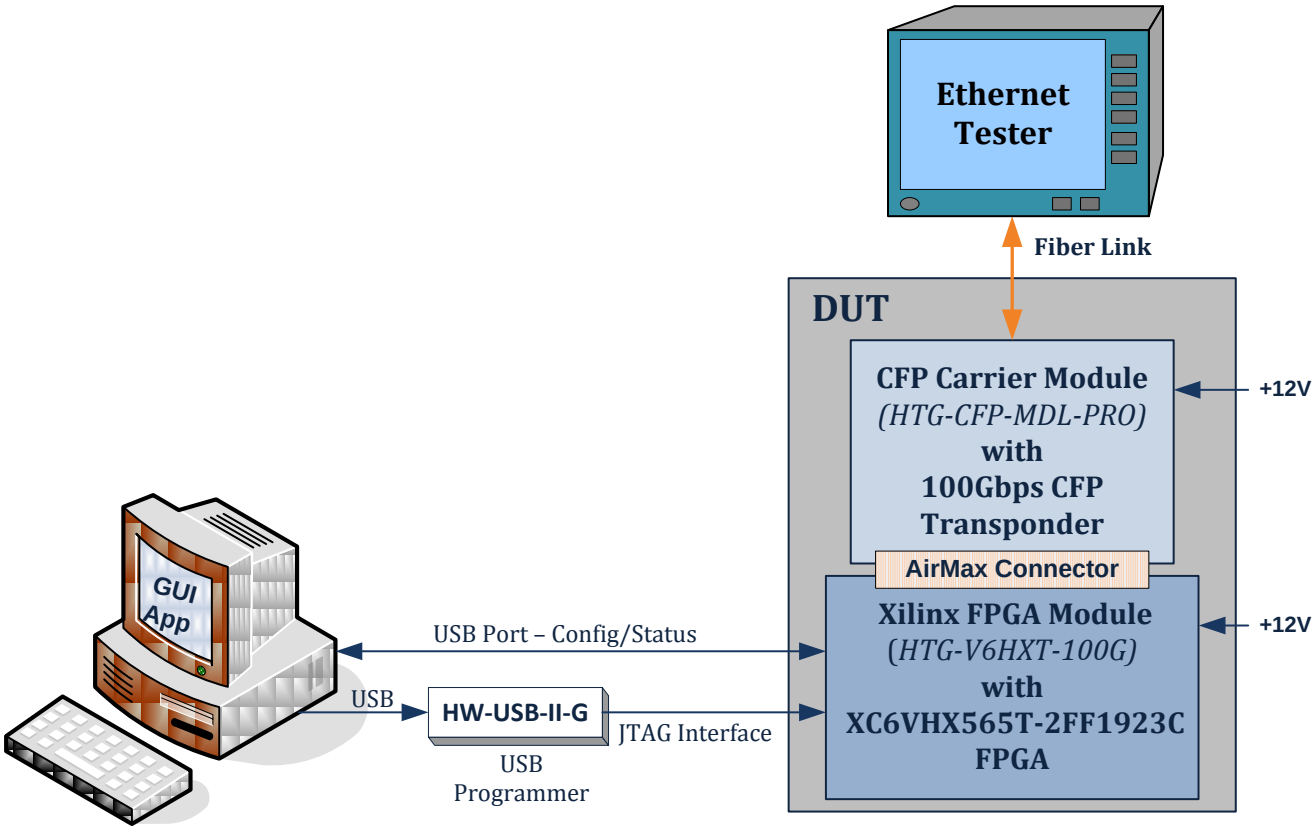


Figure 2. Elements of the Verification Test Setup

Following figure shows details of the FPGA elements of the DUT. The UART interface from the FPGA connects to an external USB-UART converter. A Linux or Windows host (through a USB port) running the GUI application is used to configure and control the 100G Ethernet, I2C and MDIO interfaces.

PCS core in the FPGA module connects to the CFP carrier module via the AirMax connector using the CAUI interface (ten 10.3125Gbps lanes). CFP optical transponder (plugged into the CFP carrier module) then connects to the Ethernet tester via optical cable.

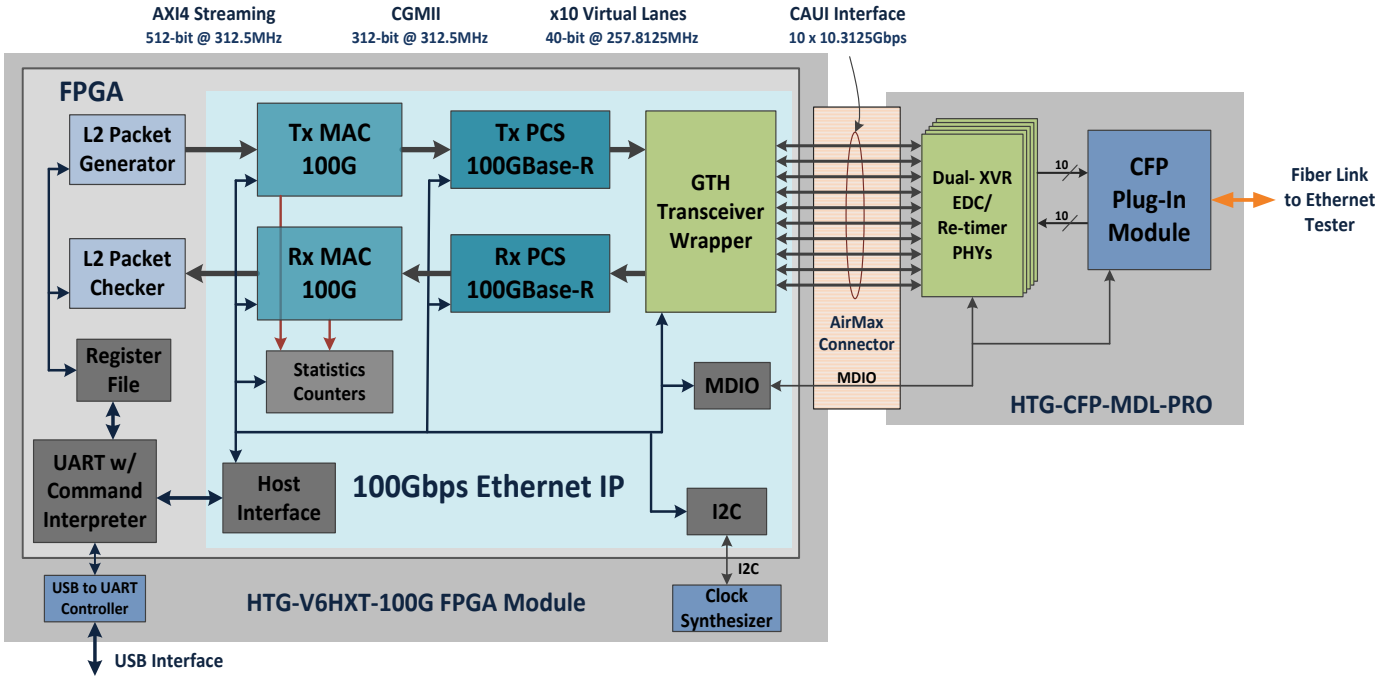
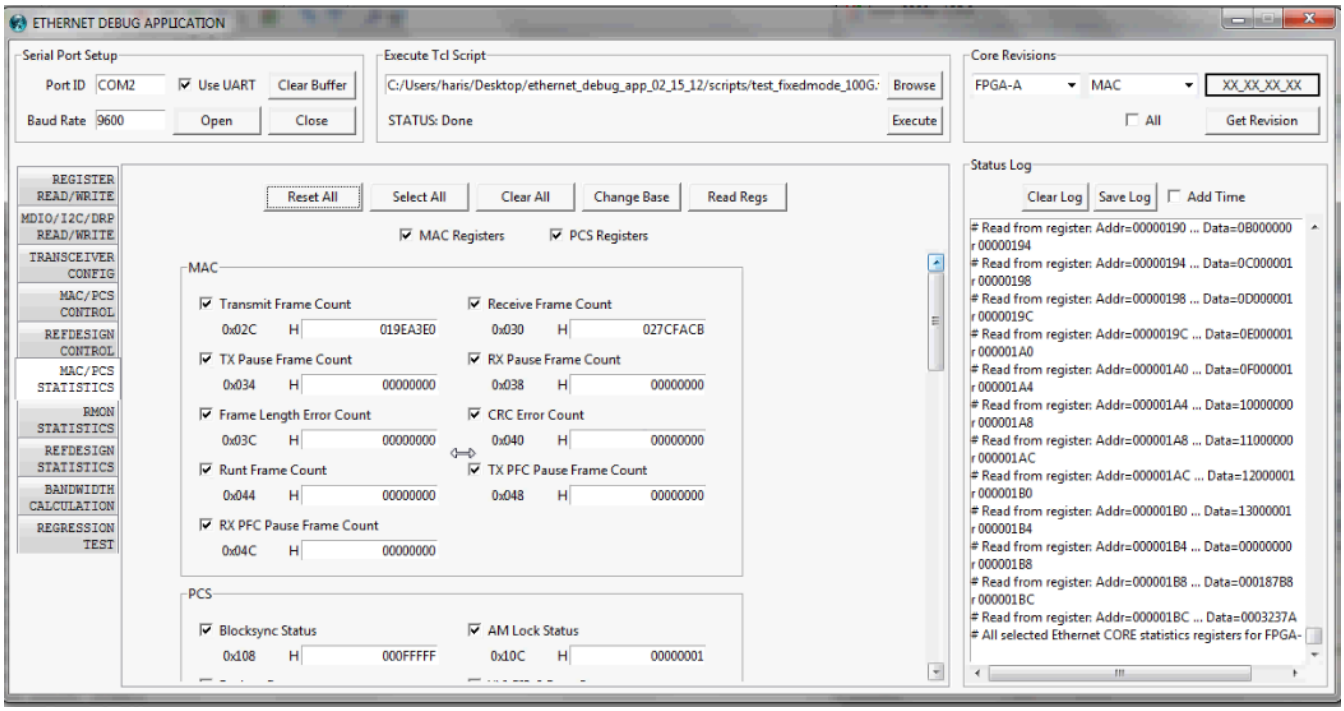


Figure 3. Details of the DUT logic blocks and interfaces

For 100G interoperability and verification tests, GUI application uses 100Gbps packet generator/checker inside the FPGA to generate and check MAC frames up to full line rate. The packet generator supports a basic rate control mechanism to control the packet/data rate on the interface. The generator can be configured for fixed size as well as pseudo random packet size packet transmission. An incrementing counter is used as payload for the MAC frames. The checker on the receive side verifies the payload of receive MAC frames and reports error in the payload.

A comprehensive set of transmit and receive counters in the MAC core provide a detailed view of the packet statistics including various error types.

Following is a snapshot for the GUI application for the L2 packet test results screen.



2. INTEROPERABILITY TESTS

Test # and Description	Case #	Results
INTOP-1.1 — Ethernet Layer-1 interoperability	I	PASS
	II	PASS
	III	PASS
	IV	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT achieves basic L1 synchronization. I. Verify that the DUT achieves block synchronization on all lanes. II. Verify that the DUT achieves Alignment Marker (AM) lock on all lanes. III. Verify that the DUT doesn't indicate any BIP-8 parity errors. IV. Verify that the DUT doesn't indicate any BER errors.		
Comments		

Test # and Description	Case #	Results
INTOP-1.2 — Ethernet Layer-2 interoperability (Fixed length packets)	I	PASS
	II	PASS
	III	PASS
	IV	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT achieves basic L2 synchronization with fixed length (Nominal size) packets. I. Verify that the DUT can detect frames on the receive path. Receive packet counter should be incrementing. II. Verify that the remote device can detect frames transmitted by the DUT. Check the transmit counters in DUT and receive counters at the remote device. III. Verify that the DUT doesn't report any CRC errors, length errors or any kind of L2 packet errors. IV. Verify that the DUT doesn't report any flow control operation. Pause frame counters should be zero.		
Comments		

Test # and Description	Case #	Results
INTOP-1.3 — Ethernet Layer-2 interoperability (Random length packets)	I	PASS
	II	PASS
	III	PASS
	IV	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT achieves basic L2 synchronization with random length packets. I. Verify that the DUT can detect frames on the receive path. Receive packet counter should be incrementing. II. Verify that the remote device can detect frames transmitted by the DUT. Check the transmit counters in DUT and receive counters at the remote device. III. Verify that the DUT doesn't report any CRC errors, length errors or any kind of L2 packet errors. IV. Verify that the DUT doesn't report any flow control operation. Pause frame counters should be zero.		
Comments		

3. EHERNET PCS (LAYER-1) TESTS:

Test # and Description	Case #	Results
PCS-1.1 — PCS BIP-8 error insertion and reporting	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can detect and report BIP-8 errors inserted by the remote device. I. Verify that the DUT can detect and report BIP-8 errors on all virtual lanes. II. Verify that the DUT can detect and report BIP-8 errors inserted on individual lanes.		
Comments		
- Single error and a burst of known number of errors were inserted from the test equipment.		

Test # and Description	Case #	Results
PCS-1.2 — PCS sync header error insertion and reporting	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can detect and report sync header errors on all the virtual lanes I. Verify that the DUT can detect and report consecutive sync header errors on all virtual lanes. The inserted sync header errors should not bring the lane out of blocksync (lane gets out of sync when 65 invalid sync headers are received in a 1024 sync window). Try up to maximum 64 invalid sync headers and observe that the PCS doesn't go out of sync. II. Verify that the DUT can detect sync header errors when the remote device inserts invalid sync headers at random times. Increase the errors up to the BER indication (97 invalid 66-bit sync headers are detected within a 500µs window for 100GBASE-R, or a 1.25ms window for 40GBASE-R).		
Comments		

Test # and Description	Case #	Results
PCS-1.3 — Handling of receive clock difference compensation	I	**PASS**
	II	**PASS**

Expected Results & Test Case Descriptions

Purpose: To verify that the DUT can properly compensate for the clock differences in both positive and negative directions.

I. Verify that the DUT can compensate for positive clock PPM differences as required by the IEEE specifications.

II. Verify that the DUT can compensate for negative clock PPM differences required by the IEEE specifications.

Comments

- IEEE specifications require a maximum of +/-100 ppm clock tolerance for the receiving station. This translates into +200 and -200 maximum clock compensation requirement on the receiver if the oscillators at the transmitting and receiving ends are at their extremes. During this test, the clock difference between the DUT and testing station increased up to 250 – 260 ppm in each direction without any errors reported by any of the devices. The test was run with standard maximum packet size of 1518 bytes.
- Clock differences of up to 200 ppm were also checked for jumbo frames (10K bytes).
- Clock differences of up to 200 ppm were also checked for random size packets ranging from 64B to 10K jumbo frames.

4. ETHERNET MAC (LAYER-2) TESTS:

Test # and Description	Case #	Results
MAC-1.1 — Reception of frames with CRC-32 errors	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can detect and report CRC-32 errors. I. Verify that the DUT can detect CRC errors (single & burst) inserted by the remote device. II. Verify that the reception of bad CRC packets doesn't affect the reception of good packets (i.e. packets with no CRC error).		
Comments		
- A known number of CRC errors were inserted from the test equipment and the CRC error count reported by the DUT was checked. The packet counter reported correct number of errors in single and burst mode CRC errors		

Test # and Description	Case #	Results
MAC-1.2 — Reception of back to back 64B frames.	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can handle 64B back to back frames with and without padding I. Verify that the DUT can handle back to back 64B frames with no padding. II. Verify that the DUT can handle back to back 64B frames with padding. Two or three payload sizes with padding should be checked.		
Comments		
- Tests were performed with different payload sizes less than or equal to 64 bytes. The size of received packets at the DUT was checked (RMON statistics). No errors were reported by the DUT.		

Test # and Description	Case #	Results
MAC-1.3 — Reception of 65B frames.	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can handle 65B back to back frames. I. Verify that the DUT can handle back to back 65B frames without any errors. This is the worst case in terms of bandwidth. II. Verify that the DUT can handle back to back "Nmod65B" frames without any errors. Example packet sizes are 130, 325, 1300 etc.		
Comments		

Test # and Description	Case #	Results
MAC-1.4 — Transmission of valid CRC frames.	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT always computes and transmits frames with proper CRC-32 field. I. Generate fixed length packets from DUT (or loopback the receive frames to transmit MAC) and verify that the remote device (testing station) doesn't report any CRC errors. Different frames sizes should be validated. II. Generate random length packets from DUT (or loopback the receive frames to transmit MAC) and verify that the remote device doesn't report any CRC errors.		
Comments		

Test # and Description	Case #	Results
MAC-1.5 — Handling of Jumbo frames	I	PASS
	II	PASS
Expected Results & Test Case Descriptions		
Purpose: To verify that the DUT can handle packets with length greater than maximum frame size (jumbo frames). I. Verify that the DUT can properly handle jumbo frames in both transmit and receive path. Use a fixed length packet size greater than the Ethernet maximum frame size. Possible lengths are 2000, 5125, 7777, or 9600 bytes. II. Verify that the DUT can handle jumbo frames when they are precede/followed by frames normal Ethernet frames (i.e. less than maximum frames size).		
Comments		

Test # and Description	Case #	Results
MAC-1.6 — Maximum bandwidth Calculation.	I	PASS
	II	PASS

Expected Results & Test Case Descriptions

Purpose: To observe and calculate the maximum L2 bandwidth achieved by the DUT for different frame lengths in both transmit and receive directions.

I. Observe the maximum bandwidth that the DUT can achieve for the following packet lengths. Also make sure that no error is reported during the test.

Packet Length	Observed Bandwidth (Testing Station to DUT) Gbps	Observed Bandwidth (DUT to Testing Station) Gbps
64 bytes	76.1903	76.1903
65 bytes	76.4704	76.4704
128 bytes	86.4863	86.4863
256 bytes	92.7534	92.7534
512 bytes	96.2404	96.2404
1,024 bytes	98.0840	98.0841
2,048 bytes	99.0326	99.0327
4,096 bytes	99.5139	99.5139
9,600 bytes	99.7918	99.7918
10,000 bytes	99.8002	99.8002

II. Also verify that the DUT reports correct statistics for the packet length 'bins' used for RMON,MIB statistics

Comments

- In order to observe the maximum throughput, packets were generated from the DUT and testing station independently at maximum possible rates. The testing station was set in 'Flooding' mode, described as the maximum possible bandwidth mode in the test equipment.
- Transmit and receive bandwidths reported above were checked at the test equipment.
- Both the DUT and testing station were brought to around '0' ppm clock difference so that the maximum bandwidths can be compared in both directions.

Test # and Description	Case #	Results
MAC-1.7 — Handling of different packet types.	I	PASS
	II	PASS
	III	PASS

Expected Results & Test Case Descriptions

Purpose: To verify the DUT can handle different packet types.

I. Verify that the DUT can handle VLAN tagged frames with fixed/random packet lengths.
II. Verify that the DUT can handle Ethernet type/DIX frames (frames with length field greater than 1536) with fixed/random packet lengths.
III. Verify that the DUT can handle VLAN-Type (Type/DIX VLAN tagged frames) frames with fixed/random packet lengths.

Comments

- The testing station also supported Q-in-Q frames generation. These packets were also generated and verified (No errors reported and MAC indicated them as VLAN frames) at the DUT. Further processing is higher layer functionality.

Test # and Description	Case #	Results
MAC-1.8 — Handling of packets with different kinds of destination addresses.	I	PASS
	II	PASS
	III	PASS

Expected Results & Test Case Descriptions

Purpose: To verify that the DUT can handle all kinds of destination MAC addresses.

I. Verify that the DUT can handle and report both transmit and receive Unicast packets.
II. Verify that the DUT can handle and report both transmit and receive Multicast packets.
III. Verify that the DUT can handle and report both transmit and receive Broadcast packets.

Comments

- Unicast, Multicast and Broadcast packets were generated from both DUT and the testing station and counters were checked at both the devices for the type of packets received.

Test # and Description	Case #	Results
MAC-1.9 — Transmit and receive missed or replicated packets tests.	I	PASS

Expected Results & Test Case Descriptions

Purpose: To verify that the DUT doesn't miss or replicate any packets in the receive direction and the DUT packet counters report as expected.

I. Verify that the DUT doesn't miss or replicate packets in the receive direction and valid packet counter in the DUT report correctly. For this test, a known number of packets are generated from the testing station for the different packet lengths and transmit (at the testing station) and receive (at DUT) packet good packet counters are compared. The same test is then performed for the other direction to verify the transmit path of the DUT.

Packet Length	Result
64 bytes	OK*
65 bytes	OK
128 bytes	OK
256 bytes	OK
512 bytes	OK
1,024 bytes	OK
2,048 bytes	OK
4,096 bytes	OK
9,600 bytes	OK
10,000 bytes	OK
Radom size packets	OK

Comments

* Transmit and receive packet counters matched exactly at both the testing station and DUT.

Test # and Description	Case #	Results
MAC-1.10 — Handling of PAUSE frames	I	**PASS**
	II	**PASS**

Expected Results & Test Case Descriptions

Purpose: To verify that the DUT can handle PAUSE frames in both transmit and receive direction.

III. Verify that the DUT can generate PAUSE frames in the transmit direction.

IV. Verify that the DUT can recognize PAUSE frames properly in the receive direction.

Comments

- Multiple PAUSE frames were generated by the DUT on the transmit path at random times using the host based PAUSE frame generation feature of the core. Number of PAUSE frames generated by the DUT was compared with the PAUSE frames reported by the testing station.