



Low Latency 10G (LL-10G) Ethernet Solution Competitive Analysis

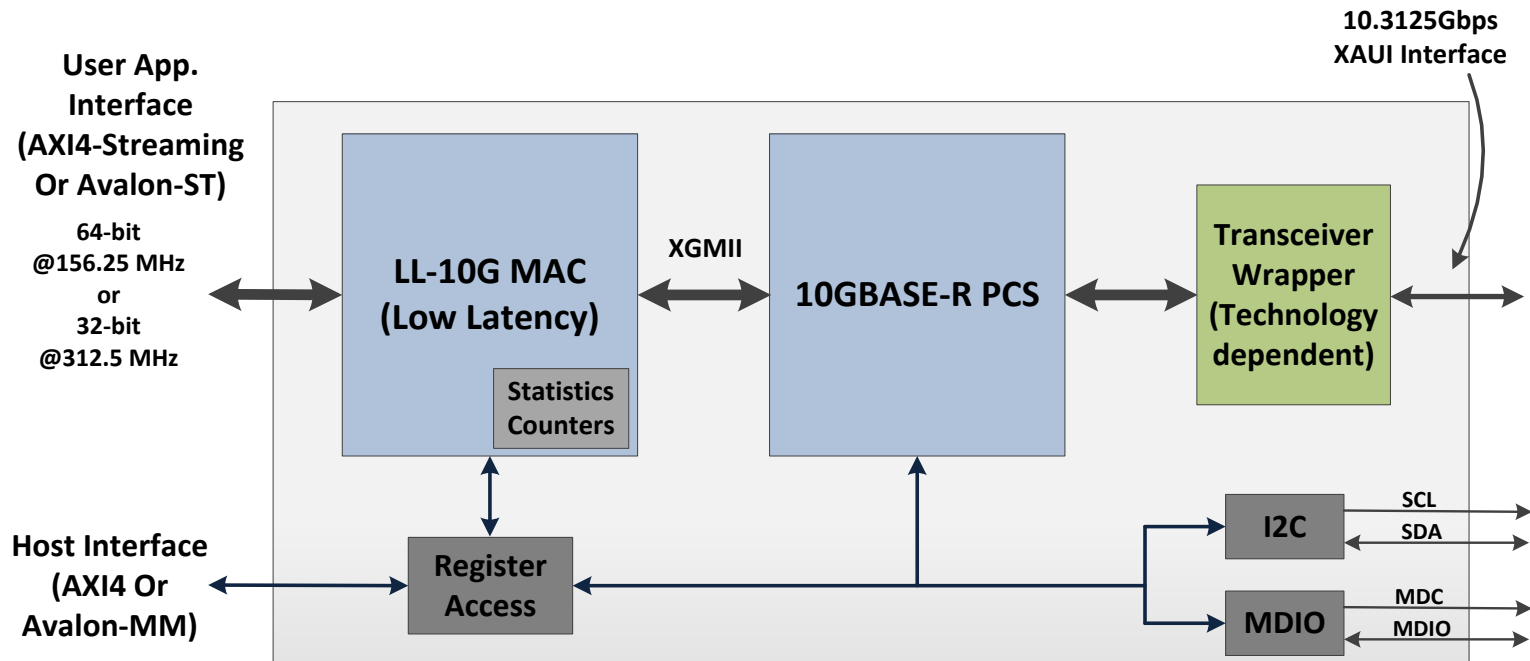
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(Revision 2.1)

10G Ethernet Solution



- Includes all the required blocks for a complete 10G Ethernet solution
- Low latency 10G (LL-10G) MAC implementation with and without management statistics counters
- Includes technology dependent transceiver wrappers (with example placement and timing constraints), MDIO and I2C blocks for communication to the optical modules.



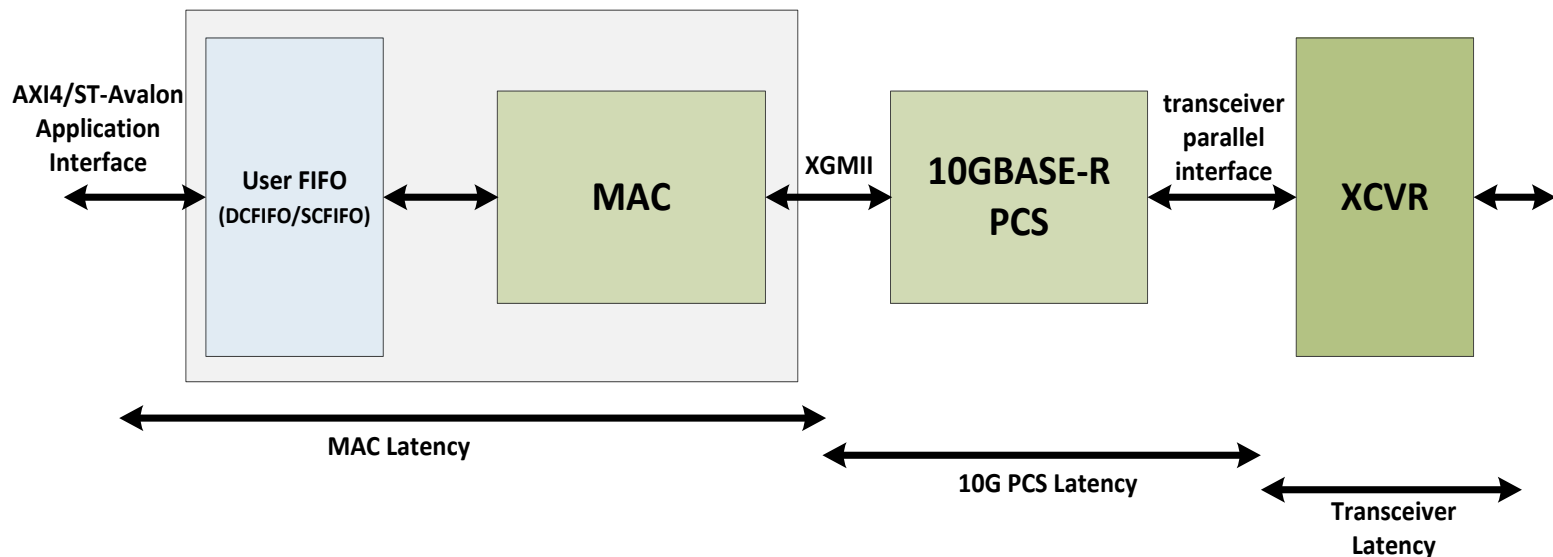
Core Highlights



- Lowest latency 10G Ethernet compared to other core solutions available from competition
- Low latency and utilization achieved through a narrow internal data path running at 312.5 MHz
- User (Application) interface support for 64-bit (@156.25 MHz) and 32-bit (@312.5 MHz) AXI4 streaming or Avalon streaming interface.
- Regressively verified solution on hardware and verified for interoperability with other devices

Latency Definitions

- MAC latency is from the first bit at the user interface to the first bit at the XGMII interface and vice versa
- 10GBASE-R latency is from the first bit at the XGMII interface to the first bit at the technology dependent (Altera/Xilinx) transceiver parallel interface
- Transceiver latency is technology dependent and always have a fixed latency for a particular device



MAC Latency Comparison (LL-10G vs Comp-X 10G)

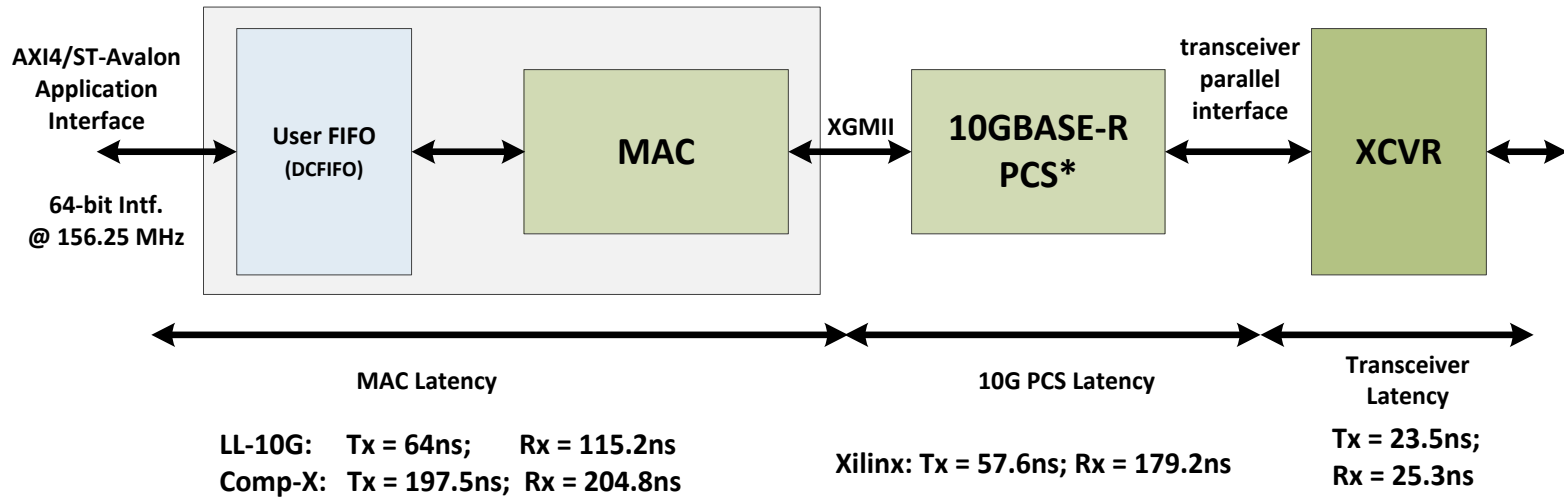


	LL-10G Latency (ns)				Comp-X Latency (ns)	
	64-bit User Interface		32-bit User Interface		64-bit User Interface only	
	Tx	Rx	Tx	Rx	Tx	Rx
MAC + DCFIFO	64	115.2	57.6	83.2	197.5*	204.8*
MAC + SCFIFO	45	83.2	41.6	76.8	--	--

* Latency values are calculated from simulations of the Comp-X 10-Gigabit Ethernet MAC v11.2 core FIFO example design (ug773, October 2011). Comp-X core datasheet provides latency for only the MAC without application interface FIFO.

- 64-bit User interface operates @156.25 MHz whereas, the 32-bit user interface operates @312.5 MHz
- DCFIFO = Dual-Clock FIFO; SCFIFO = Single clock FIFO

10G Latency (Comp-X Devices)



TOTAL LATENCY

	<u>Tx</u>	<u>Rx</u>
LL-10G:	145.1ns	319.7ns
Comp-X:	278.6ns	409.3ns

* Xilinx Provides free of charge 10GBASE-R PCS

- Total Latency based on Xilinx 10GBASE-R PCS.

MAC Latency Comparison (LL-10G vs Comp-A 10G)

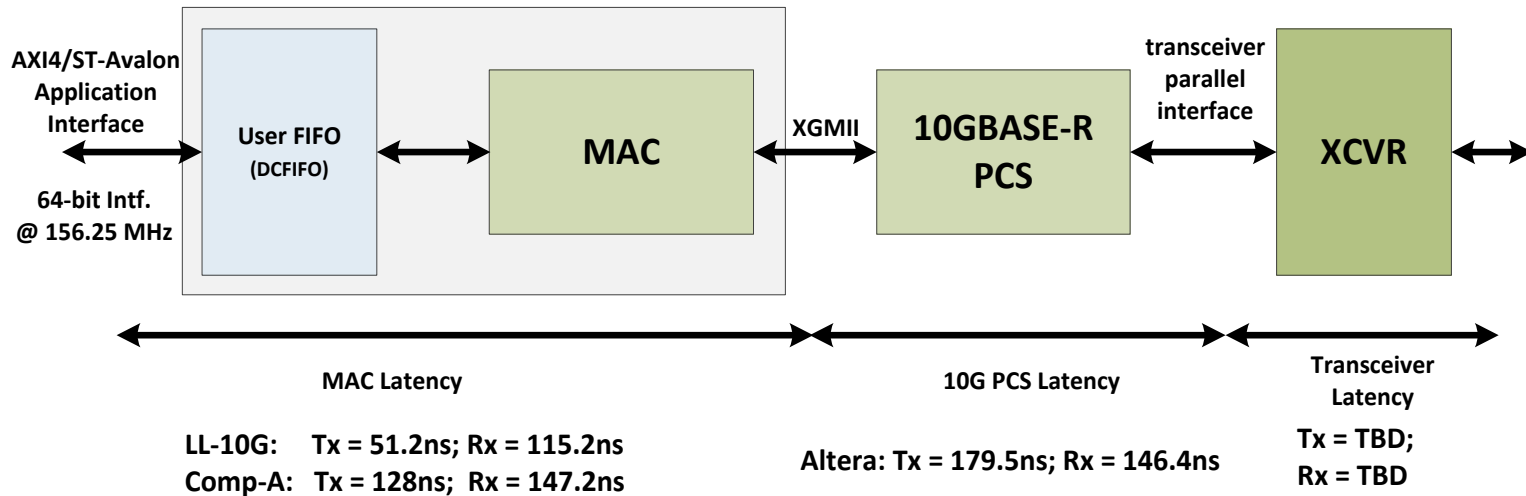


	LL-10G Latency (ns)				Comp-A Latency (ns)	
	64-bit User Interface		32-bit User Interface		64-bit User Interface	
	Tx	Rx	Tx	Rx	Tx	Rx
MAC + DCFIFO	51.2	115.2	48	83.2	128	147.2
MAC + SCFIFO	44.8	83.2	41.6	76.8	102.4	121.6

* Latency values are extracted from the Comp-A 10G MAC user guide (UG-01083-2.0, May 2011). It provides latency values including the application interface FIFO (DCFIFO/SCFIFO)

- 64-bit User interface operates @156.25 MHz whereas, the 32-bit user interface operates @312.5 MHz
- DCFIFO = Dual-Clock FIFO; SCFIFO = Single clock FIFO

10G Latency (Altera Devices)



TOTAL LATENCY

	<u>TX</u>	<u>RX</u>
LL-10G:	230.7ns*	261.6ns*
Comp-A:	307.5ns*	293.6ns*

* XCVR latency To be added

- Total Latency based on Altera's 10GBASE-R PCS.

MAC Utilization Comparison (LL-10G vs Comp-X 10G)



Virtex-6 (-2 speed)	MAC utilization (w/o RMON & MDIO)		MAC utilization (RMON & MDIO)	
	LL-10G	Comp-X	LL-10G	Comp-X
Slices	1069	1525	2152	1993
Slice LUTs	3438	3152	4587	4047
Slice Regs.	3289	3191	4843	4107
LUTRAM	50	146	185	414
BRAM(36k)	2	8	2	8

- Utilization numbers for LL-10G core are based on register based statistics counters. (Comp-X core implements LUTRAM based statistics counters)
- Utilization numbers for Comp-X 10G MAC referenced from Comp-X 10-Gigabit Ethernet MAC v11.2 core datasheet (ds813, October 2011)
- LL-10G Core implements additional features like programmable CRC and pad bytes forwarding, hash based multicast filtering, broadcast frame forwarding etc. (Refer to core datasheets for details on the features implemented). Most features not supported by Comp-X MAC core

MAC Utilization Comparison (LL-10G vs Comp-A 10G)



Stratix-IV (-2 Speed)	MAC utilization (w/o RMON & MDIO)		MAC utilization (RMON & MDIO)	
	LL-10G	Comp-A	LL-10G	Comp-A
Comb. ALUTs	2797	3133	3798	8,135
Logic Regs.	2463	3778	4545	10,117
M9k	9	13	9	13
BRAM(36k)	2	8	2	8

- Utilization numbers are based on register based statistics counters (32-bit) for both LL-10G and Comp-A cores.
- Utilization numbers for Comp-A core referenced from 10G MAC user guide (UG-01083-2.0, May 2011)

Disclaimer



- All competitive results are derived using the publicly available Comp-X and Comp-A information as of Dec 2011
- Hitek bears no responsibility to the accuracy of the latency and utilization numbers for Comp-X and Comp-A
- Latency and utilization numbers may change with the updates to the cores by all vendors