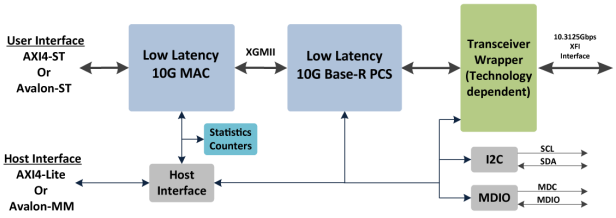
Low Latency 10G Ethernet IP Solution

Product Brief (HTK-LL10G-ETH-32-FPGA)

The 10Gbps 32-bit Ethernet IP solution offers a fully integrated IEEE802.3-2015 compliant package for NIC (Network Interface Card) and Ethernet switching applications. This extremely low latency solution is specifically targeted for demanding financial, high frequency trading and HPC applications. As shown in the figure below, the 10Gbps Ethernet IP includes: Ultra-Low latency MAC; Tx = 12.4ns, Rx = 15.5ns; (32-bit user interface mode with FCS generation and checking)

- Low latency MAC; Tx = 50.0ns, Rx = 70.4ns; (32- bit user interface mode)
- Low latency PCS; Tx = 77.1ns, Rx = 121.3ns; (32- bit user interface mode)
- Flexible 10GBase-R PCS options with XFI interface for direct SFP+/XFP attachment
- Technology dependent transceiver wrapper for Altera and/or Xilinx FPGAs
- Statistics counter block (for RMON and MIB) MDIO and I2C cores for external module and optical module status/control



A complete reference design using a L2 (MAC level) packet generator/checker is also included to facilitate quick integration of the Ethernet IP in a user design. A GUI application interacts with the reference design's hardware elements through a UART interface (a PCIe option is also available). An application (with optional basic Linux PCIe driver/API) is also provided for memory mapped read/write access to the internal registers. See Appendix A for details.

MAC core is designed with 32-bit data path operating at 312.5MHz to take advantage of high-performance fabrics of the 28nm and 20nm FPGAs. This implementation approach also delivers industry's lowest latency and low area footprint.

As the PCS and transceiver wrapper is included with the Ethernet IP solution, the line side directly connects the 10.3125Gbps FPGA transceiver to the optical module (SFP+, XFP etc).

Ethernet IP solution implements two user (application) side interfaces. The register configuration and control port is a 32-bit AXI4-Lite or Avalon-MM interface. Depending upon the application layer, user can select a 32-bit @312.5MHz or 64-bit @ 156.25MHz AXI-4 Streaming or Avalon Streaming bus to interface with the MAC block.

10Gbps Ethernet IP supports advanced features like per-priority pause frames (compliant with 802.3bd specifications) to enable Converged Enhanced Ethernet (CEE) applications like data center bridging that employ IEEE 802.1Qbb Priority Flow Control (PFC) to pause traffic based on the priority levels.

Features Overview (Mac Core)

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively.
- Implements 802.3bd specification with ability to generate and recognize PFC pause frames.
- Implements reconciliation sublayer functionality with start and terminate control characters alignment, error control character and fault sequence insertion and detection.
- Multiple user interface options for the MAC data path: AXI-4 or Avalon streaming with 32-bit data path at 312.5MHz or 64-bit data path at 156.25MHz
- PCS layer XGMII interface implemented as 64-bit (single data rate) SDR interface at 156.25MHz for direct interface to 10GBase-R, XAUI and RXUAI cores
- Deficit Idle Count (DIC) mechanism to ensure data rates of 10Gbps at the transmit interface.
- Optional padding of frames if the size of frame is less than 64 bytes.
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention. Non-PFC Mode only.
- Pause frame generation additionally controllable by user application offering flexible traffic flow control.
- Support for VLAN tagged frames according to IEEE 802.1Q.
- Support any type of Ethernet Frames such as SNAP / LLC, Ethernet II/DIX or IP traffic.
- Discards frames with mismatching destination address on receive (except Broadcast and Multicast frames).
- Programmable Promiscuous mode support to omit MAC destination address checking on receive path.
- Optional multicast address filtering with 64-bit Hash Filtering table providing imperfect filtering to reduce load on higher layers.

- High speed CRC-32 generation and checking. Optional prevention of CRC appending in frame data by MAC to allow CRC to be pre-embedded in frame data by user application.
- Optional insertion of error control character in transmitted frame data.
- Optional forwarding of the CRC field to user application interface.
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames).
- Status signals available with each Frame on the user interface providing information such as frame length, VLAN frame type indication and error information.
- Optional padding termination on RX path for NIC applications or forwarding of unmodified data to the user interface.
- Optional internal XGMII Loop-back.
- Statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames.
- Altera Avalon or Xilinx AXI4 interface compliant user (FIFO) interface.
- Transmit and Receive FIFOs with configurable depths having a default depth of 1KB/512B (128 64-bit/32-bit words) each, according to user interface bus width.
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.
- For devices without the support for the 10.3125Gbps transceivers, Ethernet IP solution can be configured to operate with vendor specific XAUI and RXAUI cores.

PCS Core Features

- Implements 10GBase-R PCS core compliant with IEEE 802.3-2008 Specifications.
- Implements a 64-bit XGMII interface to operate at 156.25MHz for 10G Ethernet.
- Implements 64b/66b encoding/decoding for transmit and receive PCS using 802.3-2008 specified control codes.
- Implements 10G scrambling/descrambling using 802.3-2008 specified polynomial 1 + x39 + x58.
- Implements 66-bit block synchronization state machine as specified in 802.3-2008 specifications.
- Implements Inter Packet Gap (IPG) insertion/deletion for clock compensation while maintaining a minimum of 5 bytes IPG.
- Implements gear-box logic to convert 66-bit blocks to 40-bit for line side. The 40-bit interface operates at the transceiver reference clock. There is an option with Xilinx 7-series devices to use the gear-box logic available in the transceiver. In this case, the gear-box logic in PCS is bypassed and the 66-bit blocks are presented at line side operating at the transceiver reference clock.
- Implements Bit Error Rate (BER) monitor for monitoring excessive error ratio. In addition, the core implements various status and statistics required by the IEEE 802.3-2008 such as block synchronization status and test mode error counter.
- Implements optional XGMII remote loopback to loopback data received from Rx PCS back to Tx PCS.

Deliverables

- Encrypted MAC and PCS RTL for simulation and synthesis
- Encrypted L2 packet generator and checker RTL for simulation and synthesis
- Source code RTL (Verilog) for top level Ethernet wrappers to allow for user specific customizations.
- Technology specific transceiver wrappers for the selected device family
- Source code RTL (Verilog) for AXI4-Lite and Avalon- MM arbiters and address decoders
- Constraint files and synthesis scripts for design compilation
- Linux based APIs/tools to access core configuration and statistics registers
- Design guide(s) and user manual(s)

Links

http://hiteksys.com/fpga-ip-cores/10g-low-latency-ethernet

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Resource Utilization

The utilization summary of the 10G Ethernet solution is given in following tables. The utilization numbers are best in class as compared to other available 10G Ethernet cores with comparable feature set.

The Ethernet solution has been fully verified on different hardware platforms for both Altera and Xilinx FPGAs and has also been verified for interoperability with other 10G capable devices.

10G LL Ethernet IP - Resource Usage for Xilinx Devices

Device	*User Interface (AXI4-ST)*	*Priority Flow Control (PFC)*	*Slice LUTS*	*Slice Registers*	*BRAMs*
UltraScale/ UltraScale+	32-Bit	No	*5,365*	*5,822*	*18K = 2; 36K = 3*
		Yes	*5,567*	6,344	*18K = 2; 36K = 3*
	64-Bit	No	*5,570*	6,079	*18K = 0; 36K = 5*
		Yes	*5,773*	6,601	*18K = 0; 36K = 5*
7-Series	32-Bit	No	*5,523*	*5,822*	*18K = 2; 36K = 3*
		Yes	*5,728*	6,344	*18K = 2; 36K = 3*
	64-Bit	No	*5,705*	6,079	*18K = 0; 36K = 5*
		Yes	*5,926*	6,601	*18K = 0; 36K = 5*
Virtex 6	32-Bit	No	*6,509*	*5,781*	*18K = 2; 36K = 3*
		Yes	6,708	6,303	*18K = 2; 36K = 3*
	64-Bit	No	6,696	6,104	*18K = 0; 36K = 5*
		Yes	6,902	6,626	*18K = 0; 36K = 5*

Note:

- *These utilization numbers include MAC and PCS Register files.*
- *Register based RMON statistics block adds additional 1948 LUTs and 1807 registers.*

10G LL Ethernet IP - Resource Usage for Altera Devices

Device	*User Interface Width*	*Priority Flow Control (PFC)*	*COMB. ALUTs*	*Registers*	*Memory*
Arria 10	Avalon, 32-Bit	No	4,909	6,057	M20K = 8
		Yes	5,114	6,607	M20K = 8
	Avalon, 64-Bit	No	4,942	6,261	M20K = 10
		Yes	5,174	6,807	M20K = 10
Stratix V	Avalon, 32-Bit	No	4,906	6,035	M20K = 8
		Yes	5,111	6,586	M20K = 8
	Avalon, 64-Bit	No	4,939	6,243	M20K = 10
		Yes	5,171	6,766	M20K = 10
Stratix IV	Avalon, 32-Bit	No	4,939	5,656	M9K = 9
		Yes	5,135	6,176	M9K = 9
	Avalon, 64-Bit	No	4,977	5,839	M9K = 11
		Yes	5,204	6,360	M9K = 11

Note:

- *These utilization numbers include MAC and PCS Register files.*
- *Register based RMON statistics block adds additional 2003 LUTs and 1808 registers.*