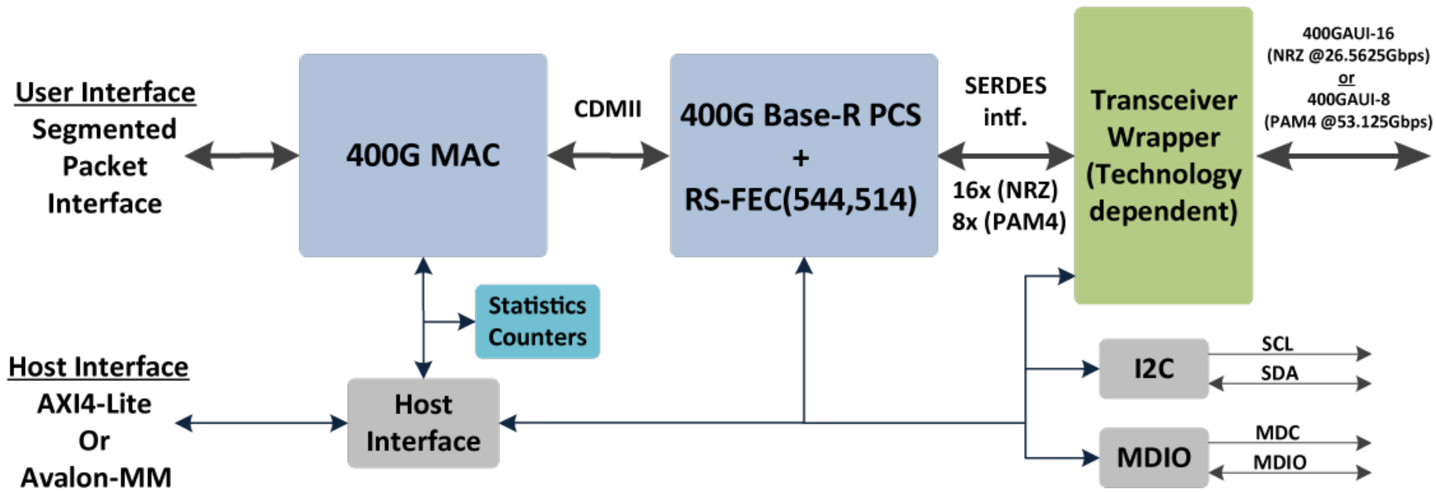
400 Gigabit Ethernet IP

Product Brief (HTK-400G-ETH-FPGA)



The 400Gbps Ethernet IP solution offers a fully integrated IEEE802.3bs compliant solution for use in core networks, Ethernet switching and network interface card (NIC) applications. The Ethernet cores implement an efficient architecture to achieve best in class resource utilization and performance numbers for targeting the complete 400Gbps Ethernet solution to ASICs as well as FPGAs.

As shown in figure, the 400Gbps Ethernet IP solution includes:

- 400GBase-R PCS core with RS-FEC(544,514) KP4 FEC.
- 400Gbps MAC core with streaming user interface.
- Technology dependent transceiver wrappers for NRZ/ PAM4 SERDES transceivers.
- RMON block for statistics counters.
- Synthesizable packet generator/checker for quick bring up and standalone verification of 400G Ethernet solution.
- AXI4-Lite or Avalon-MM based fabric for host interface register access.
- Linux based APIs/tools for configuration of the 400G Ethernet cores and getting various statistics.
- MDIO and I2C cores for optical module control and status.

PCS Core Features

- Implements 400GBase-R PCS core compliant with IEEE 802.3bs specifications.
- Implements Reed Solomon FEC (RS-FEC) encoder, error correction and decoder compliant to 802.3bs Clause 119 with (544,514) code words at full 400Gbps line speed.
- Implements 257b transcoding in RS-FEC sublayer.
- Implements 16x26.5625Gbps (NRZ) and 8x53.125Gbps (PAM4) line side SERDES interfaces.
- Implements periodic insertion of Alignment Marker (AM) on the transmit path and deletion on the receive path.
- Implements lane reordering and deskew to align all PCS lanes and assemble an aggregate 400Gbps CDMII stream.
- Implements 1024bit 400Gbps CDMII interface for seamless connection to 400Gbps MAC.
- Implements 64b/66b encoding and decoding for transmit and receive PCS respectively.
- Implements 400G PCS scrambling and descrambling compliant to 802.3 polynomial 1 + x39 + x58.
- Implements Inter Frame Gap (IFG) Insertion/Deletion for clock compensation elastic buffers.
- Implements optional remote CDMII loopback mode which directs received CDMII traffic to transmit path.
- Implements various configuration, status and statistics registers accessible through standard AXI4-Lite or Avalon-MM host interface.

MAC Core Features

- Implements full 802.3 standard MAC layer with preamble/ SFD generation, CRC-32 generation and checking on transmit and receive paths respectively.
- Implements Deficit Idle Count (DIC) mechanism to ensure maximum possible throughput for transmit MAC while maintaining 12byte average Inter Frame Gap (IFG)

- Implements RS layer functionality with start and terminate control characters alignment, error control character and fault sequence insertion and detection.
- Implements a 1024bit 400G CDMII interface.
- Supports minimum 64byte packet for transmit MAC and discards all frames less than 64bytes on receive MAC.
- Implements CRC-32 generation and checking at full 400Gbps rate.
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention. Non PFC mode only.
- Implements optional pause frame generation from user application interface for traffic flow control.
- Implements 802.3bd Priority Flow Control (PFC) support.
- Implements support for standard IEEE Ethernet length/type, 802.1Q VLAN tagged length/type and pause frames
- Implements destination MAC address checking on receive path and accepts Unicast frames with matching destination MAC address only.
- Implements programmable promiscuous mode to accept all incoming traffic.
- Implements programmable broadcast and multicast frames filtering on receive path.
- Implements programmable maximum frame length support for standard Ethernet and Jumbo frames.
- Implements length error checking for standard Ethernet length frames and truncation of frames greater than programmed maximum frame length.
- Implements optional internal MII loopback support to direct transmit traffic back to MAC receive path.
- Implements sideband channel to provide per frame information to the user application on MAC receive path.
- Implements multiple statistics counters and per frame events for transmit and receive path such as good frames, CRC error, length error, remote/local fault etc.
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.
- Implements streaming user application interface.
- Implements Avalon-MM or AXI4-Lite host interface to access core's internal registers.

Deliverables

- Encrypted MAC and PCS RTL for simulation and synthesis
- Encrypted L2 packet generator and checker RTL for simulation and synthesis
- Source code RTL (Verilog) for top level Ethernet wrappers to allow for user specific customizations.
- Technology specific transceiver wrappers for the selected device family
- Source code RTL (Verilog) for AXI4-Lite and Avalon-MM arbiters and address decoders
- Constraint files and synthesis scripts for design compilation
- Linux based APIs/tools to access core configuration and statistics registers
- Design guide(s) and user manual(s)

Resource Utilization

Resource utilization is provided under NDA. Contact sales for more information.

Validated/Ported Module List

1. Intel Stratix 10 TX Signal Integrity Development Kit; Stratix 10 TX 280 FPGA with E-Tile Transceivers capable of up to 57.8Gbps PAM4 / 28.9Gbps NRZ, QSFP-DD optical module interface.

(https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kits-s10-tx-si.html)

Product Ordering Codes

HTK-400G-ETH-FPGA: Complete MAC + PCS solution
HTK-400G-PCS-FPGA: PCS only option

Links

https://hiteksys.com/fpga-ip-cores
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