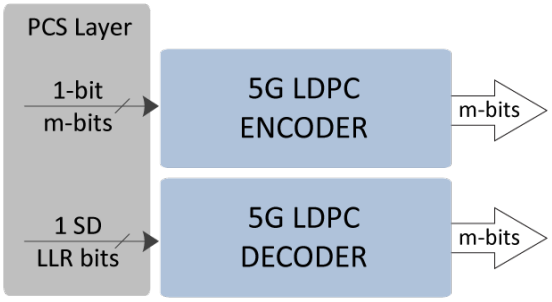
5G LDPC IP Core Solution

Product Brief (HTK-5G-LDPC)

The 5G LDPC IP core implements Low-density parity-check (LDPC) codes compliant with the 3rd Generation Partnership Project (3GPP) 5G specifications. LDPC codes are linear error correcting codes used to transmit and receive messages over noisy channels. The LDPC IP core is designed to comply with the 3GPP TS 38.212, Release 15 specifications.

Polar and LDPC codes have been adopted as the newer physical layer channel coding schemes in 5G New Radio (NR) access technology standards by 3GPP. The drivers for this selection comes from three main 5G usage scenarios of enhanced mobile broadband(eMBB), ultra-reliable and low latency communications (URLLC) and massive machine type communications (mMTC), which require improved throughput, latency, and reliability compared with a 4G system. 5G LDPC codes are designed to support high throughput, a variable code rate and length and hybrid automatic repeat request (HARQ) in addition to good error correcting capability. LDPC codes are primarily adopted for data channels while Polar codes are adopted for control channels.



The 5G NR LDPC codes supports a variety of configurations, based on the three parameters: lifting size, Z or m, code rate, R and base graph. The high number of variations requires many base matrices to aid in the encoding and decoding processes. They are stored intelligently to reduce on-chip memory usage. The encoder takes in the hard decision input bits, attaches the parity to the data information bits and outputs the encoded code word as m-bits per cycle. The decoder takes in noisy code words, encoded as soft decision symbols and decodes it iteratively until maximum iterations are consumed or the correct decoding condition is achieved.

Features Overview

- Supports per block configurable block length, code rate, base graph, and maximum number of iterations
- Supports serial or semi-parallel input/output hard decision bits interface for LDPC encoder
- Supports serial or semi-parallel input/output soft decision interface for LDPC encoder
- Supports 5-bit or 6-bit LLR soft decision precision
- Supports a maximum of 255 iterations for LDPC decoder
- Supports early exit of decoding operation based on syndrome check after each iteration
- Implements Low Latency decoder ensuring high throughput

Deliverables

- Encrypted RTL for simulation and synthesis
- System Verilog based test-bench
- Matlab/Octave behavioral model
- Golden test vectors from standard
- User Documentation

Resource Utilization

Resource utilization is provided under NDA. Contact sales for more information.

Ordering Information

HTK-5GNR-LDPC: 5G NR LDPC Encoder and Decoder
HTK-5GNR-LDPC-ENC: 5G NR LDPC Encoder only
HTK-5GNR-LDPC-DEC: 5G NR LDPC Decoder only

Links

https://hiteksys.com/fpga-ip-cores
https://hiteksys.com/fpga-ip-cores/5gnr-ldpc

For sales or more information:

Hitek Systems LLC
Phone: +1-301-528-8074
Email: sales@hiteksys.com