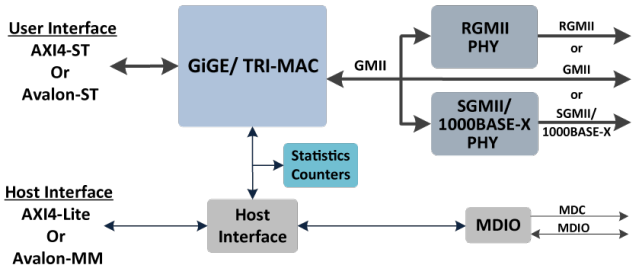
GiGE/Triple-Speed MAC

Product Brief (HTK-GIGE-TRI-MAC-8)

The GiGE/Triple-speed Ethernet MAC offers an IEEE802.3-2015 compliant solution that meets the requirements for GiGE/tri-mode LAN in NIC (Network Interface Card) applications.

As shown in figure, the GiGE/Triple-Speed MAC IP includes:

- AXI4-Streaming or Avalon-Streaming, FIFO based user side interface
- Supports only 1000Mbps speed with GMII/RGMII PCS side interface
- Supports 10/100/1000Mbps speed in SGMII mode with PCS/PMA IP Cores from Xilinx and Altera
- Statistics counter block (for RMON and MIB)
- MDIO cores for external PHY status/control



A complete reference design using a simple L2 (MAC level) packet generator/checker is also included to facilitate quick integration of the Ethernet MAC in a user design.

MAC core is designed with 8-bit data path operating at 1.25, 12.5, and 125MHz for 10Mbps, 100Mbps and 1000Mbps Ethernet modes respectively. Ethernet IP solution implements two user (application) side interfaces. The register access port is a 32-bit AXI4- Lite or Avalon-MM interface. The Ethernet user application interface is provided through 32-bit FIFOs with a simple handshake mechanism. FIFO clock interface is fixed at 125MHz clock rate for all modes of operation.

Features Overview

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively.
- Dynamically configurable to support 10Mbps, 100Mbps or 1000Mbps operation in SGMII mode
- Seamless interface to commercial Ethernet PHY device via an 8-Bit GMII or 4-Bit RGMII interface operating at 125MHz for GiGE mode
- Connects to GBIC/SFP module or SGMII PHY through PCS/PMA IP core.
- Pause frame generation additionally controllable by user application for traffic flow control • Support for VLAN tagged frames according to IEEE 802.1Q.
- Support any type of Ethernet Frames such as SNAP/LLC, Ethernet-II/DIX and VLAN tagged frames.
- Programmable MAC address filtering; discards frames with mismatching destination address on receive (Except Broadcast and frames)
- Programmable Promiscuous mode support to omit MAC destination address checking on receive Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing FIFO Based User Interface AXI4-ST Or Avalon-ST Host Interface AXI4-Lite Or Avalon-MM SGMII MDC MDIO load
- Optional multi-cast address filtering with 64-bit HASH Filtering table providing imperfect filtering to reduce load on higher layers
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Status word available with each Frame on the user interface providing information such as frame length, VLAN frame type indication and error information
- Optional padding termination on RX path for NIC applications or forwarding of unmodified data to the user interface
- Internal GMII interface Loop-back
- Statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames
- Simple handshake user application FIFO interface with programmable threshold levels ensuring data rates of 1Gbps with full back-to-back frame transfer support
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.

MAC Resource Utilization

The MAC core contains two configurable depth FIFOs on both TX and RX user interfaces, for frame buffering. The following table provides the resource utilization for the Tri-MAC with 1KB FIFO depths.

The Tri-MAC core has been fully verified on different hardware platforms for both Altera and Xilinx FPGAs.

Tri-MAC - Resource Usage for Xilinx Devices

Device	*Slice LUTS*	*Slice Registers*	*BRAMs*
UltraScale/ Ultrascale+	1,733	2,064	*18K = 1; 36K = 1*
7-Series	1,744	2,063	*18K = 1; 36K = 1*

Tri-MAC - Resource Usage for Altera Devices

Device	*Combinational ALUTS*	*Registers*	*Memory (M20K)*
Arria 10	1,379	1,753	2
Stratix V	1,381	1,705	2

Deliverables

- Encrypted MAC and PCS RTL for simulation and synthesis
- Encrypted L2 packet generator and checker RTL for simulation and synthesis
- Source code RTL (Verilog) for top level Ethernet wrappers to allow for user specific customizations.
- Technology specific transceiver wrappers for the selected device family
- Source code RTL (Verilog) for AXI4-Lite and Avalon-MM arbiters and address decoders
- Constraint files and synthesis scripts for design compilation
- Linux based APIs/tools to access core configuration and statistics registers
- Design guide(s) and user manual(s)

Links

http://hiteksys.com/fpga-ip-cores/gige-triple-speed-ethernet-mac

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