



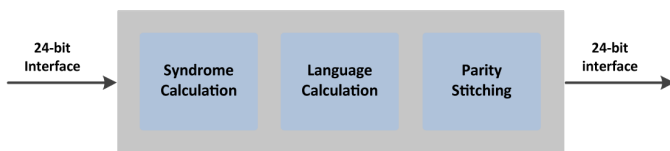
# Reed-Solomon FEC IP Solution

## Product Brief (HTK-RSFEC-N255-K239)

The Reed-Solomon Forward Error Correction (RS-FEC) IP solution implements the RS-FEC sublayer defined in IEEE 802.3 and ITU-T standards. The design is targeted for applications requiring high performance, high throughput and low logic utilization.

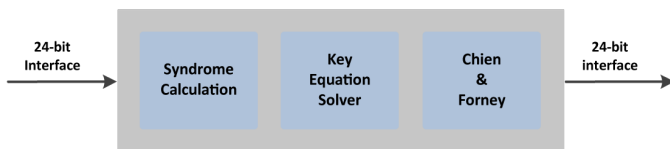
### Features Overview

#### RS-FEC Encoder Features



- Implements RS-FEC encoder with efficient Syndrome and Lagrange calculation blocks
- High through-put, low latency encoder processes 3 symbols in parallel.
- Implements RS-FEC (N=255,K=239,m=8) encoder with polynomial specified by IEEE 802.3 and ITU-T specifications
- Valid based implementation allows discontinuous data flow and/or bandwidth-controlled operation

#### RS-FEC Decoder Features



- Implements RS-FEC decoder with efficient Syndrome, KES, Chien and Forney calculation blocks
- Implements RS-FEC (N=255,K=239,m=8) decoder with polynomial specified by IEEE 802.3 and ITU-T specifications
- Valid based implementation allows discontinuous data flow and/or bandwidth-controlled operation
- Statistics for correctable and uncorrectable code words

### Deliverables

- Encrypted RTL for simulation and synthesis
- Encoder/decoder test-bench using vectors

### Resource Utilization

Resource utilization is provided under NDA. Contact sales for more information.

### Product Ordering Codes

HTK-RSFEC-N255-K239: RS-FEC Encoder/Decoder  
HTK-RSFEC-ENC-N255-K239: RS-FEC Encoder only  
HTK-RSFEC-DEC-N255-K239: RS-FEC Decoder only

### Links

<https://hiteksys.com/fpga-ip-cores>

<https://hiteksys.com/fpga-ip-cores/reed-solomon-fec>

### For sales or more information:



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