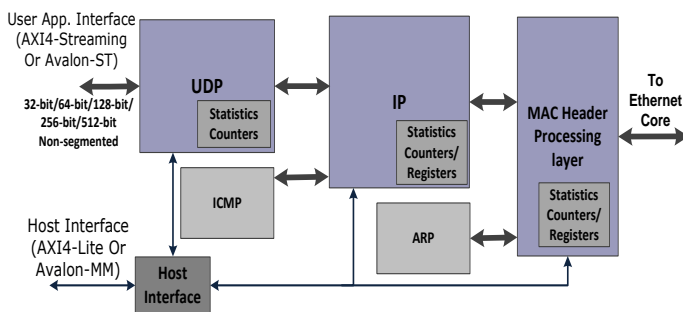


UDP/IP Offload Engine (UOE)

Product Brief (HTK-UOE-FPGA-aaa)

UOE is high performance and highly customizable UDP/IP hardware stack compliant with RFC 768 (for UDP) and RFC 791 (for IPv4)/RFC 2460(for IPv6). As shown in the figure below, the UOE core includes:

- L4 UDP engine
- L3 IPv4/IPv6 engine
- L2 Mac engine
- Statistic counter blocks and user configurable registers
- ARP and ICMP buffers



UOE is designed to be integrated with any Ethernet Solutions that has AXI4-ST/Avalon-ST interface. User interface can be customized for AXI4-ST or Avalon-ST. Data path in addition supports a wide range of interface widths from 32-bit up to 512-bit. Single clock design provides easy manageability for the user.

32-bit user interface runs @ 312.5MHz clock for 10G, 64-bit user interface runs @ 156.25MHz for 10G, 128-bit user interface runs @ 312.5MHz for 40G, 256-bit user interface runs @ 156.25MHz for 40G, and 512-bit user interface runs @ 312.5MHz for 100G.

Core IP layer can be customized for IPv4 or IPv6 depending on the application.

The header fields can be configured once for point-to-point applications.

Our solution implements and delivers the low latency with highest throughput and minimum or no inter-packet gap.

Key Features

- Implements RFC 768 for UDP.
- Implements RFC 791 for IPv4.
- Implements RFC 2460 for IPv6.
- Supports 32/64/128/256/512-bit wide data paths.
- Can handle data rate up to 100Gbps.
- Multiple user interface options for the data path; AXI4 streaming or Avalon Streaming
- Supports for VLAN tagged frames according to IEEE 802.1Q.
- Supports user data packets from 1 to 1472 bytes in standard mode.
- Optional Jumbo frames support up to 9000 bytes.
- High performance core with low latency and lowest inter-packet gaps.
- Remove padding from MAC frames.
- Discard datagrams having MAC errors, e.g. CRC error, PHY error.
- Can distinguish between unicast /multicast /broadcast datagrams and discard multicast packets.
- UDP checksum generation and checking at high speed using an efficient pipelined implementation.
- IPv4 checksum generation and checking and discard datagrams if checksum fails.
- Filtering of received frames based on MAC and IP address.
- Encapsulation/De-Encapsulation of MAC header along with UDP and IP
- Can send ARP Announce and ARP Response Packets
- Classify ARP and IP packets at L2
- Classify UDP and ICMP packets at L3
- Customizable IP layer for version 4 and 6.
- Can discard IP datagrams with invalid fragment offsets flags.
- Forward fragmented IP datagrams to fragment buffer after UDP and IP checksum checking and IP header sanity checks.
- Drops datagrams with invalid IP header fields.
- Implements statistics of frames, datagrams, segments at L2, L3 and L4 respectively.

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Resource Utilization

The UOE core utilization summary is given in following tables.

UOE - Resource Usage for Xilinx Devices

<i>Device</i>	<i>User Interface (AXI4-ST)</i>	<i>Jumbo Frames Support</i>	<i>Slice LUTs</i>	<i>Slice Registers</i>	<i>BRAMs</i>
UltraScale/ UltraScale+	32-Bit	No	5,256	7,786	18K = 15; 36K = 3
		Yes	5,359	7,843	18K = 11; 36K = 19
	64-Bit	No	6,189	9,179	18K = 11; 36K = 8
		Yes	6,283	9,236	18K = 11; 36K = 20
	128-Bit	No	7,961	11,764	18K = 11; 36K = 14
		Yes	8,054	11,821	18K = 11; 36K = 22
	256-Bit	No	12,096	16,972	18K = 8; 36K = 26
		Yes	12,176	17,011	18K = 11; 36K = 26
	512-Bit	No	20,202	29,613	18K = 14; 36K = 43
		Yes	20,250	29,630	18K = 17; 36K = 43

UOE - Resource Usage for Intel Devices

<i>Device</i>	<i>User Interface (Avalon-ST)</i>	<i>Jumbo Frames Support</i>	<i>COMB. ALUTs</i>	<i>Registers</i>	<i>Memory Blocks</i>
Arria 10	32-Bit	No	4,685	7,543	M20K = 22
		Yes	4,760	7,658	M20K = 46
	64-Bit	No	5,315	8,689	M20K = 28
		Yes	5,385	8,763	M20K = 48
	128-Bit	No	6,648	10,799	M20K = 40
		Yes	6,723	10,874	M20K = 52
	256-Bit	No	9,745	14,632	M20K = 58
		Yes	9,812	14,741	M20K = 58
	512-Bit	No	14,807	23,692	M20K = 96
		Yes	14,850	23,719	M20K = 96

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Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Intel) compiled (synthesized netlist) binary
- Other licensing options include:
 - Vendor and device family agnostic source code (Verilog) license

Ordering information

Following table lists the ordering code for the UOE IP Core.

UOE – Ordering Codes

<i>Part #</i>	<i>Description</i>
HTK-UOE-FPGA-32	32-bit data path UDP/IP core @ 312.5MHz clock for 10Gbps interface
HTK-UOE-FPGA-64	64-bit data path UDP/IP core @ 156.25MHz clock for 10Gbps interface
HTK-UOE-FPGA-128	128-bit data path UDP/IP core @ 312.5MHz clock for 40Gbps interface
HTK-UOE-FPGA-256	256-bit data path UDP/IP core @ 156.35MHz clock for 40Gbps interface
HTK-UOE-FPGA-512	512-bit data path UDP/IP core @ 312.5MHz clock for 100Gbps interface

Contact and Sales Information

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