PCI Express Block DMA/SGDMA IP Solution

Product Brief (HTK-BLK-SGDMA-FPGA)

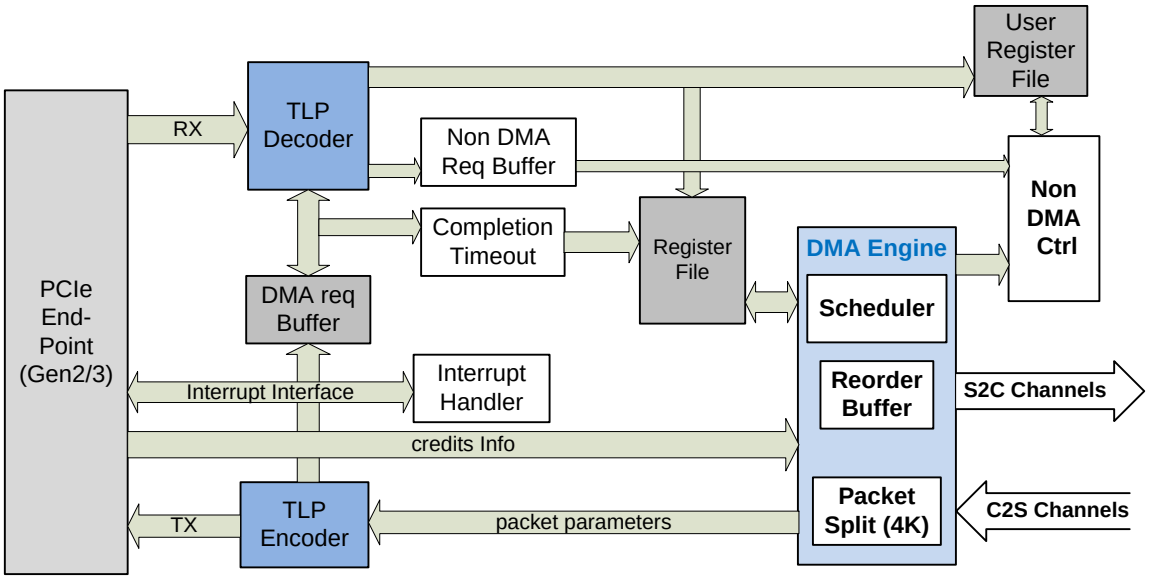
The PCI-Express DMA core offers a fully integrated, flexible and highly optimized solution for high bandwidth and low latency direct memory access between host memory and target FPGAs. An optional Scatter-Gather DMA mode is supported for efficient utilization of the host memory.

The core supports PCIe Gen2 and Gen3 capable endpoints for both Xilinx and Altera devices. It implements a single clock domain 64bit, 128bit or 256bit design depending on the Endpoint generation (Gen2/3) and user interface width. The core provides a standard AXI4-S compliant user interface and has a multichannel support. An efficient scheduler is implemented to provide even priority to all channels which are scheduled in a round robin fashion.

A simple block DMA variation of the core is available in which data is transferred to/from a continuous buffer in host memory. A variation of the block DMA core, Direct DMA, is available where the C2S transfers are completely managed by the user interface at the DMA core. For this mode, C2S transfer address, size and interrupt information can be provided directly by the user using the TUSER field in the AXI4-S interface. The interrupt can be enabled for each packet or after multiple packets for interrupt coalescing as required by user application. For S2C transfers, the host memory address and size information is provided to user application using the TUSER field.

A high performance scatter-gather variation of the core is also available to support multiple scattered system buffers with packet markers (start and end of packet and other packet fields). This mode is highly suitable with packet user logic for example Ethernet cores.

The DMA core also provides optional performance instrumentation logic that can help user to monitor the maximum and minimum throughput states for performance intensive applications.



Key Features

- Supports PCIe Gen1, Gen2 and Gen3
- Support 64-bit, 128-bit and 256-bit Xilinx and Altera's Endpoints
- AXI4-Streaming compliant user interface
- Supports multiple independent DMA channels
- Each channel supports block or scatter-gather mode of operation depending on the core variation
- High performance core with minimum latency and very low inter-packet gaps
- Credits based transfer allows maximum efficient use of available bandwidth
- Dynamic 32-bit and 64-bit systems address support
- Support up to 4096 descriptors in Scatter-Gather mode. The descriptors are generated in a continuous buffer on the host memory by the DMA driver for efficient fetching/update of descriptors by the DMA core
- Supports page size of up to 2 Megabytes
- Supports dynamic Maximum Read Request Size (MRRS), Read Completion Boundary (RCB) and Maximum Payload Size (MPS). Updates to these parameters can be made by writing to the Endpoint configuration registers from PCIe driver
- Supports reordering of received completions from PCIe root complex in S2C direction
- Implements packet splitter logic to split the transfers at 4K boundary in C2S direction as required by PCIe specifications
- Supports MSI and Legacy Interrupts
- Per channel DMA Interrupt Enable/Disable support
- Provides a simple register file read/write interface for accessing user application registers
- Implements optional internal Completion timeout counters and DMA performance counters
- Implements soft reset logic to reset the DMA engines to known good state
- Includes efficient Linux (32/64 bit) PCIe and DMA drivers with example applications for DMA transfers.
- Includes self-checking simulation test-benches with support for Endpoint bypass for faster simulations
- Includes PCIe DMA reference design with data generator/checker on the FPGA side and C/C++ based user application on host side

Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Altera) compiled (synthesized netlist) binary
- Additional vendor license provided at only 50% cost of the base license. This allows for cost effective multi-vendor designs with identical user and control interfaces.
- Other licensing options include:
  - Vendor and device family agnostic source code (Verilog) license

Contact and Sales Information

For further information, contact sales representative at:

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Resource Utilization

The utilization summary of the PCIe DMA solution is given in following tables. The utilization numbers vary based on the different variations of the core. The solution has been fully verified on different hardware platforms for both Altera and Xilinx FPGAs and for different host platforms.

PCIE DMA IP - Resource Usage for Xilinx Devices

Device	*Datapath Width*	*Core Variation*	*Channels*	*Slice LUTS*	*Slice Registers*	*BRAMs*
UltraScale/ UltraScale+	256-bit	Block DMA	2	10228	11143	*36K = 13; 18K = 14*
			4	18800	17025	*36K = 22; 18K = 24*
			8	36266	29325	*36K = 44; 18K = 44*
		Scatter-Gather DMA	2	9839	11052	*36K = 24; 18K = 14*
			4	19335	17603	*36K = 48; 18K = 24*
			8	36339	29174	*36K = 89; 18K = 43*
UltraScale/ UltraScale+	128-bit	Block DMA	2	7807	9583	*36K = 15; 18K = 13*
			4	13627	152124	*36K = 34; 18K = 21*
			8	25126	25896	*36K = 64; 18K = 37*
		Scatter-Gather DMA	2	7154	9695	*36K = 40; 18K = 15*
			4	13532	15312	*36K = 56; 18K = 25*
			8	24559	25774	*36K = 109; 18K = 44*
7-Series	256-bit	Block DMA	2	10281	11141	*36K = 13; 18K = 14*
			4	19356	17571	*36K = 26; 18K = 24*
			8	36879	29329	*36K = 44; 18K = 44*
		Scatter-Gather DMA	2	9908	11091	*36K = 24; 18K = 14*
			4	19356	17616	*36K = 48; 18K = 24*
			8	37287	29312	*36K = 89; 18K = 43*
7-Series	128-bit	Block DMA	2	7874	9583	*36K = 15; 18K = 13*
			4	13736	15118	*36K = 34; 18K = 21*
			8	25403	25882	*36K = 64; 18K = 37*
		Scatter-Gather DMA	2	7195	9732	*36K = 28; 18K = 15*
			4	13491	15319	*36K = 56; 18K = 25*
			8	24865	25746	*36K = 109; 18K = 44*

Note:

- *Scatter-Gather DMA utilization includes memory to maintain scatter-gather list fetched from host*

Deliverables

- Compiled synthesizable binaries or encrypted RTL for the DMA core
- Self-checking behavioral models and test benches for simulation
- Constraint files and synthesis scripts for design compilation
- Linux driver; ***Source Code***
- Reference design with integrated PCIe endpoint, data generator/checker and software user application
- Design guide(s) and user manuals
- USA based technical support by developers